UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/817,270 | 03/27/2001 | Ryoichi Inanami | 03180.0278 | 7690 |

22852 7590 05/07/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| JOHNSTON, PHILLIP A | |
| ART UNIT | PAPER NUMBER |
| 2881 | |

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/817,270 | INANAMI ET AL. | |
| | Examiner | Art Unit | |
| | Phillip A Johnston | 2881 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Detailed Action***

***Examiners Response to Arguments***

1. Claims 1-21, as amended are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,250,812 to Murai, in view of Watanabe, U.S. Patent No. 6,335,898, and in further view of Shibata, U.S. Patent No. 5,371,373. for the reasons given in First Office Action (Paper No. 6).

2. Applicant's arguments filed 3-12-2003 have been fully considered but they are not persuasive.

3. Applicants argument 1

Applicant states that "The Examiner alleged that Murai's repetitive unit patterns correspond to the standard cells as claimed and that Murai's aperture corresponds to the character projection aperture (Office Action, p. 4). Applicants, however, submit that the Examiner has misconstrued Murai. The charged beam exposure as claimed delineates patterns to describe a system in a logic expression and converts the logic expression into a connection of standard cells, and the standard cells are expressed in shaping holes of the character projection aperture. In contrast, the apertures of Murai's second aperture plate represent repetitive patterns, not standard cells. These patterns are determined by dividing design data into random patterns and repetitive patterns. Murai, col. 4, lines 11-21 The repetitive patterns are then resized into various sizes

and then formed onto aperture plate 210. Murai, Fig. 10B and col. 7, line 57 to col. 8, line 19. Thus, Murai's apertures correspond to repetitive patterns of various sizes, not standard cells associated with logic expressions. Therefore, Murai fails to teach or suggest at least a charged beam exposure for delineating patterns of a system on a substrate to describe the system in a logic expression, to convert the logic expression into a connection of standard cells, and to delineate patterns of the standard cells on the substrate comprising, inter alia, "a Character Projection (CP) aperture having shaping holes of the charged beam having shapes of the standard cells."

4. Response to Applicants argument 1.

Regarding the Examiners implication that “Murai's repetitive unit patterns correspond to the standard cells as claimed and that Murai's aperture corresponds to the character projection aperture (Office Action, p. 4)”.

The Applicant is respectfully directed to page 5, line 15 of Applicants specification, which states ‘Here “standard cell” means a pattern defined in the cell library’.

The applicant is also respectfully directed to Murai (812), Column 4, line 11-27, which states; The CAD data is stored in, for example, a memory 215 (see FIG. 2). In general, the CAD data includes data of non-repetitive patterns (or random patterns) and data of repetitive patterns having unit patterns repeated at a coordinate and a pitch designated. In step 32, only the repetitive patterns are extracted from the CAD data. Also Column 4, line 41-45, which states; In step 34, the computer 213 processes

the repetitive pattern data to determine the shape and size of each of repeated unit patterns which form an aperture and the number of the repeated unit patterns in the aperture in each of a longitudinal direction and a lateral direction.

The examiner has interpreted from a comparison of the Murai (812) references above to the Applicants statements above, that the unit pattern of Murai (812) and the "Standard Cell" as defined by the Applicant, are the same.

5. Applicants argument 2.

Applicant states that, "Moreover, Watanabe fails to teach or suggest these claim elements. Watanabe is directed to a semiconductor chip having a data input/output lines and a logic circuit integrated on a single chip. Watanabe discloses the design schematic of the semiconductor chip. See Watanabe, Figs. 1 and 2. However, Watanabe does not disclose a method of forming the chip or a charge beam device, which could be used to form the chip. Therefore, Watanabe fails to teach or suggest at least a charged beam exposure for delineating patterns of a system on a substrate to describe the system in a ICI logic expression, to convert the logic expression into a connection of standard cells, and II' to delineate patterns of the standard cells on the substrate comprising, inter alia, "a Character Projection (CP) aperture having shaping holes of the charged beam having, shapes of the standard cells."

Thus, Murai and Watanabe, when taken alone or in combination, fail to teach or suggest all the elements of claim 1. Thus, a prima facie case of obviousness has not been established for claim 1. For at least this reason, claim 1 is allowable.

Claims 2-6 are allowable at least due to their dependence from allowable claim 1."

6. Examiners response to Argument 2.

The Applicant is respectfully directed to Watanabe (898), Column 14, line 39-51, which states; Therefore, it is possible to reduce the number of masks to be modified. Especially, in the case of a memory/logic mixed chip as in the present invention, it should be considered that there may be a need to change the capacity of the memory or the construction of the logic in accordance with the purpose of use. If several kinds of memory cores MR and basic patterns of the switch groups SWG for the transfer circuit TG are prepared as libraries beforehand from such a view-point of the purpose of use, it is possible to design masks of an LSI chip promptly by selecting necessary ones from the libraries, composing a logic portion by use of a basic library for logic, and performing the arrangement and wiring.

The applicant is further respectfully directed to Column 22, line 58-67 in Watanabe (898), which states; Thus, the number of stages of switch groups SWG can be reduced by arranging many switches SW within the pitch of I/O lines MIOi. Therefore, in the case where the pitch of I/O lines MIOi is wider, the chip size can be further reduced. It is of course that even in the case where many switches are arranged within the pitch of I/O lines MIOi, the layout design of the transfer circuit TG can be made very easy if a common portion of the layout is registered as a library beforehand.

The examiner has interpreted from the Watanabe (898) references above, that by preparing memory cores and switch groups as basic patterns and registering them

as part of the basic logic library beforehand is equivalent to creating new "standard cells" as required. In addition, the resultant construction of the logic in accordance with the purpose of use, and selecting these newly created "standard cells" from the library, is equivalent to "describing the system in a logic expression, to convert the logic expression into a connection of standard cells", as recited in amended Claims 1,7, and 15; as well as, "conducting logic synthesis using the extracted standard cells", as recited in original Claim 9. The examiner has also interpreted that reducing the mask design time is an important step in the lithography process.

7. Applicants argument 3.

Applicant states that, "Furthermore, Shibata fails to teach or suggest these claim elements. Shibata is directed to an electron lithography method. However, as in Murai, Shibata teaches that the lithography patterns are separated according to repetitive and non-repetitive patterns, but does not disclose standard cells associated with logic expressions. See Shibata, Fig. 1. Therefore, Shibata fails to teach or suggest at least an exposure pattern data generation apparatus or method as recited in claims 7 and 15, respectively. Thus, Murai, Watanabe, and Shibata, when taken alone or in combination, fail to teach or suggest all the elements of claims 7 and 15. Thus, a prima facie case of obviousness has not been established for claims 7 and 15. For at least this reason, claims 7 and 15 allowable."

8. Examiners response to argument 3.

The Applicant is respectfully directed to the Abstract in Shibata (373), which states; An input pattern is classified into repetitive and non-repetitive patterns. The

classified non-repetitive pattern is further classified into unit areas, i.e., repetitive and no-repetitive unit patterns. Next, the non-repetitive unit patterns are converted into lithography data, while the repetitive unit patterns and repetitive patterns are composed on the lithography data of the non-repetitive unit patterns. A result of composing the repetitive unit patterns and repetitive patterns and the lithography data of the non-repetitive unit patterns is sorted according to a lithography sequence and output as the lithography data. Thus, the repetitive unit areas are extracted from the non-repetitive patterns and processed in the same manner as the repetitive patterns to thereby reduce the number of lithography shots.

The examiner has interpreted from the reference above, as well as those in the foregoing responses, that the unit patterns in Shibata (373) are equivalent to "standard cells", as recited in Applicants Claims 1,7, and 15.

9. Applicants argument 4.

Applicant states that, " Moreover, there is no suggestion or motivation to modify Murai or Watanabe to produce Applicants' claimed invention."

Applicant also states that, "Moreover, there is no suggestion or motivation to modify Murai, Watanabe, or Shibata to produce Applicants' claimed invention."

10. Examiners response to argument 4.

The Applicant is respectfully directed to page 5, lines 17-27 of Applicants specification, which states "According to the first feature, In case of particularly

manufacturing a logic device such as an application specific IC (ASIC) or a system LSI, the shapes of patterns (or standard cells) defined in cell libraries used in a design phase are manufactured on the aperture as electron beam shaping holes and the patterns are made into characters subjected to CP exposure, whereby electron beam exposure having higher throughput than conventional throughput is realized. Further, by making the standard cells into characters subjected to CP exposure, the number of electron beam shots can be sufficiently reduced and throughput can be, therefore, improved."

The Applicant is respectfully directed to the following statements in Murai (812), Watanabe (898), and Shibata (373) which indicate that the objectives of these references are the same as those stated above by the Applicant; i.e., to reduce the number of shots and increase throughput:

In Murai (812) see Column 1, line 50; Column 2, line 61, Column 3, line 4; and Column 5, line 62.

In Watanabe (898), see Column 14, line 39-51.

In Shibata (373), see Column 1, line 60.

***Conclusion***

11. The Amendment filed on 1-03-2003 under 37 CFR 1.131 has been considered but is ineffective to overcome the Murai (812), Watanabe(898), and Shibata (373) references.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip A Johnston whose telephone number is 305 7022. The examiner can normally be reached on 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 703 308 4116. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872 9318 for regular communications and 703 872 9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

PJ
April 25, 2003

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800